# 5 T855 Fault Finding

***Caution:*** **This equipment contains CMOS devices which are susceptible to damage from static charges. Refer to Section 1.2 in Part A for more information on anti-static procedures when handling these devices.**

The following test procedures and fault finding flow charts may be used to help locate a hardware problem, however they are by no means a complete fault finding procedure. If you still cannot trace the fault after progressing through them in a logical manner, contact your nearest Tait Dealer or Customer Service Organisation. If necessary, you can get additional technical help from Customer Support, Radio Systems Division, Tait Electronics Ltd, Christchurch, New Zealand (full contact details are on page 2).

***Note 1:*** In this and following sections deviation settings are given first for wide bandwidth sets, followed by settings in brackets for mid bandwidth sets ( ) and narrow bandwidth sets [ ].

***Note 2:*** Unless otherwise specified, the term "PGM800Win" used in this and following sections refers to version 2.00 and later of the software.

Refer to Section 6 where the parts lists, grid reference index and diagrams will provide detailed information on identifying and locating components and test points on the main PCB. The parts list and diagrams for the VCO PCB are in Part E.

The following topics are covered in this section.

## 5.1 Visual Checks

Remove the covers from the T855 and inspect the PCB for damaged or broken components, paying particular attention to the surface mounted devices (SMDs).

Check for defective solder joints. If repair or replacement of components is considered necessary, refer to Section 3 of Part A.

## 5.2 Component Checks

If you suspect a transistor is faulty, you can assess its performance by measuring the forward and reverse resistance of the junctions. Unless the device is completely desoldered, first make sure that the transistor is not shunted by some circuit resistance. Use a good quality EVM (e.g. Fluke 75) for taking the measurements (or a 20k ohm/V or better multimeter, using only the medium or low resistance ranges).

The collector current drawn by multi-junction transistors is a further guide to their performance.

If an IC is suspect, the most reliable check is to measure the DC operating voltages. Due to the catastrophic nature of most IC failures, the pin voltages will usually be markedly different from the recommended values in the presence of a fault. The recommended values can be obtained from either the circuit diagram or the component data catalogue.

## 5.3 Front Panel LED Indicator

The green "Supply" LED on the receiver front panel will flash according to the conditions described in the following table:

| Flash Rate | | Condition |
|---|---|---|
| fast | (⅓ sec. on/⅓ sec. off approx.) | receiver is linked with PGM800Win |
| slow | (1 sec. on/1 sec. off approx.) | VCO is out of lock - refer to Section 5.4.2 |
| unequal | (⅓ sec. on/1 sec. off approx.) | microcontroller has detected an internal communications error - refer to Section 5.7.1 |

Where two or more conditions occur at the same time, the precedence is in the order shown above (i.e. receiver linked has the highest priority, followed by VCO error, then internal error).

# 5.4 DC Checks

## 5.4.1 Power Rails

Refer to the test points & options diagrams in Section 6 for test point locations, and to the regulator fault finding chart (Section 5.7.2) for fault diagnosis.

Check the 9V (TP602) and 13.8V (TP601) power supply test points in the regulator compartment with a DMM.

Check the 20V regulator output at the test point (TP603) in the regulator compartment.

Check the 5V regulator output at the test point (TP604) in the regulator compartment and on IC310 pin 4.

Check the 5V digital regulator output at the junction of C611A (+) and IC610 pin 2 in the regulator compartment.

## 5.4.2 VCO Locking

Using a DMM, monitor the VCO control voltage on the long lead of L1 on the VCO PCB.

If the synthesiser is locked and the VCO aligned, the voltage at this point should be between 3 and 16V.

If the VCO is not locked, refer to the synthesiser fault finding charts (Section 5.7.3).

## 5.4.3 Mute Operation

The front panel "Gate" LED will show the status of the mute circuitry and will turn on when a signal is received above the threshold level.

Check that PL250 is linked correctly:

| | |
|---|---|
| noise mute | 1-2 |
| carrier mute | 2-3. |

Check that the mute gate opens as follows:

| | |
|---|---|
| noise mute - | rotate RV230 (front panel gating sensitivity) fully clockwise and check that the front panel "Gate" LED turns on; |
| carrier mute - | rotate RV235 (carrier mute) fully clockwise and check that the front panel "Gate" LED turns on. |

If the mute fails to operate correctly, refer to the noise mute fault finding chart (Section 5.7.4) or the carrier mute fault finding chart (Section 5.7.5).

# 5.5 RF Checks

## 5.5.1 VCO Frequency

Check that the VCO is phase locked (refer to Section 5.4.2).

Connect a frequency counter (level +20dBm) to the VCO input to the mixer (IC410).

Monitor the local oscillator frequency and check that it is 45MHz ***below*** the required receive frequency.

Refer to the synthesiser fault finding charts (Section 5.7.3) for further information.

## 5.5.2 RF Sensitivity

Ensure that the VCO is on the correct frequency and the receiver correctly aligned.

Check that the 12dB sinad sensitivity into the front end is as follows:

-117dBm (de-emphasised response)
-111dBm (flat response).

If the sensitivity is poor, you can trace the fault by measuring the sensitivity into successive circuit blocks. Prepare a test cable by connecting a 1nF capacitor to the end of a length of coax cable as shown in Figure 5.1.

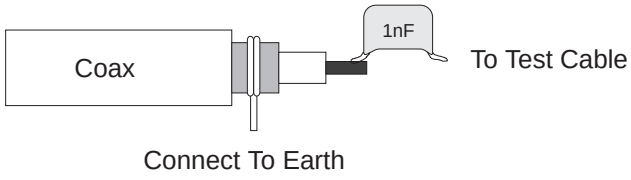



***Figure 5.1 RF Test Cable***

***Note:*** Before using the test cable, ensure the coax braid is connected to an earth point on the PCB.

Using the RF test cable, apply a modulated 45MHz signal to the test breaks in the IF section, or an on-channel RF signal to the front end test breaks.

Check that the sensitivity at each test break is within 2dB of the levels shown on the circuit diagram.

Poor sensitivity indicates a fault in one of the circuit blocks following the test break.

***Note:*** Poor sensitivity into the mixer can be caused by lack of drive level from the VCO (the drive level should be >+17dBm).

Refer to the receiver fault finding charts (Section 5.7.6) for further information.

## 5.5.3 Oscillator Stability

### 5.5.3.1 TCXO

While maintaining a low level unmodulated RF input to the receiver, loosely couple into the first IF an additional high level signal at 45MHz - you should now hear a constant low frequency beat note.

Tap the TCXO with a finger and replace it if the beat note permanently changes.

### 5.5.3.2 Second IF

While maintaining a low level unmodulated RF input to the receiver, loosely couple into the second IF an additional high level signal at 455kHz - you should now hear a constant low frequency beat note.

Adjust L385 for "zero beat".

## 5.5.4 Demodulator Output

Apply an on-channel RF signal modulated by 1kHz with ±3kHz (±2.4kHz) [±1.5kHz] deviation at an amplitude of -65dBm.

Connect an oscilloscope probe (DC coupled) to TP314 (audio output).

Check that an audio signal of approximately 800mV peak to peak is present.

Optimum tuning of the quad coil (L390) for minimum audio distortion (with a "flat" audio response) should coincide with maximum audio amplitude and a DC level of approximately 1.7V.

## 5.5.5 IF Distortion

If the audio distortion is still high after careful IF alignment (Section 3.7), sweep the IF to investigate the bandpass response.

Apply an on-channel RF signal modulated at 10Hz (sine wave) with ±12kHz (±9kHz) [±6kHz] deviation at an amplitude of -80dBm.

Connect the modulating 10Hz audio signal to the "X" input of an oscilloscope and observe the 455kHz IF input to SK320 pin 3 via a suitable RF probe on the "Y" input. Alternatively, if you have an RSSI PCB fitted, use an oscilloscope probe for the "Y" input to monitor the RSSI output voltage at pad P238 (RSSI test point) or pin 5 of D-range 1 (PL100). This will give a demodulated log response and only the top half of the wave forms shown in Figure 5.2 and Figure 5.3 will be displayed on the oscilloscope screen.

***Note:*** The "X" input should be DC coupled.

Check that the swept response has a rounded top and no sharp non-linearities (refer to Figure 5.2).

Increase the RF level to -50dBm; the trace will now show the shape of the 455kHz ceramic filter (&XF302).

Check that the response has no sharp non-linearities.

If sharp non-linearities do occur, replace the filter and sweep again to confirm a satisfactory solution (refer to Figure 5.3).

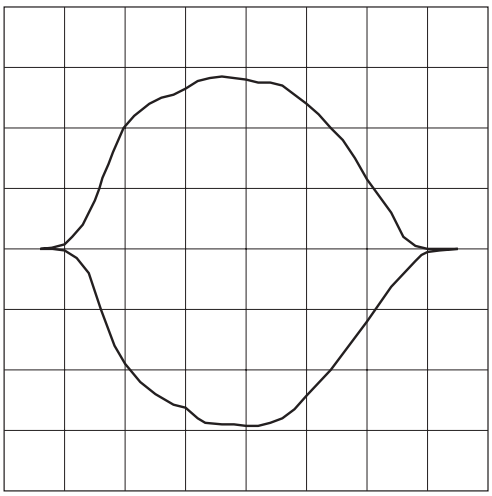


*Figure 5.2 IF Swept Response*

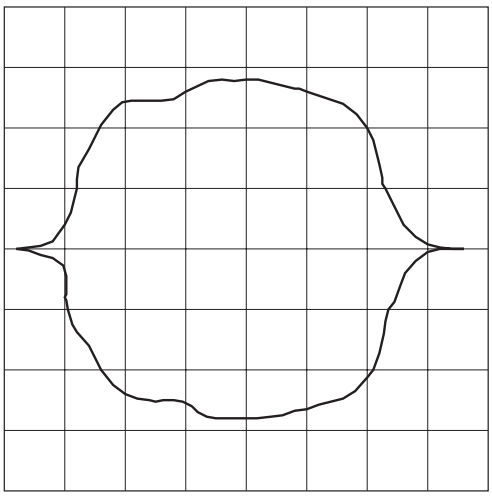


*Figure 5.3 Ceramic Filter Swept Response*

# 5.6 PGM800Win Generated Errors

The following errors are those most likely to occur using PGM800Win. Refer to the PGM800Win software user's manual for a complete list of error messages.

**Channel Switch Set**

The (programmed) default channel change was not accepted by the base station because a channel is selected externally. Try turning the external channel switch off to change the default channel in PGM800Win.

**Synth Out Of Lock**

The synthesiser received incorrect data, or the data was corrupted. Enter a frequency within the VCO switching range, or tune the VCO.

**Internal Error**

Data could not be read from the base station due to an internal error. Check for shorts or open circuits on the SDA, SCK, SYNTH and EPOT lines. The SDA, SCK and SYNTH are normally high.

**Write/Read To An Unlinked Module**

The link to the module does not exist. Undefined error.

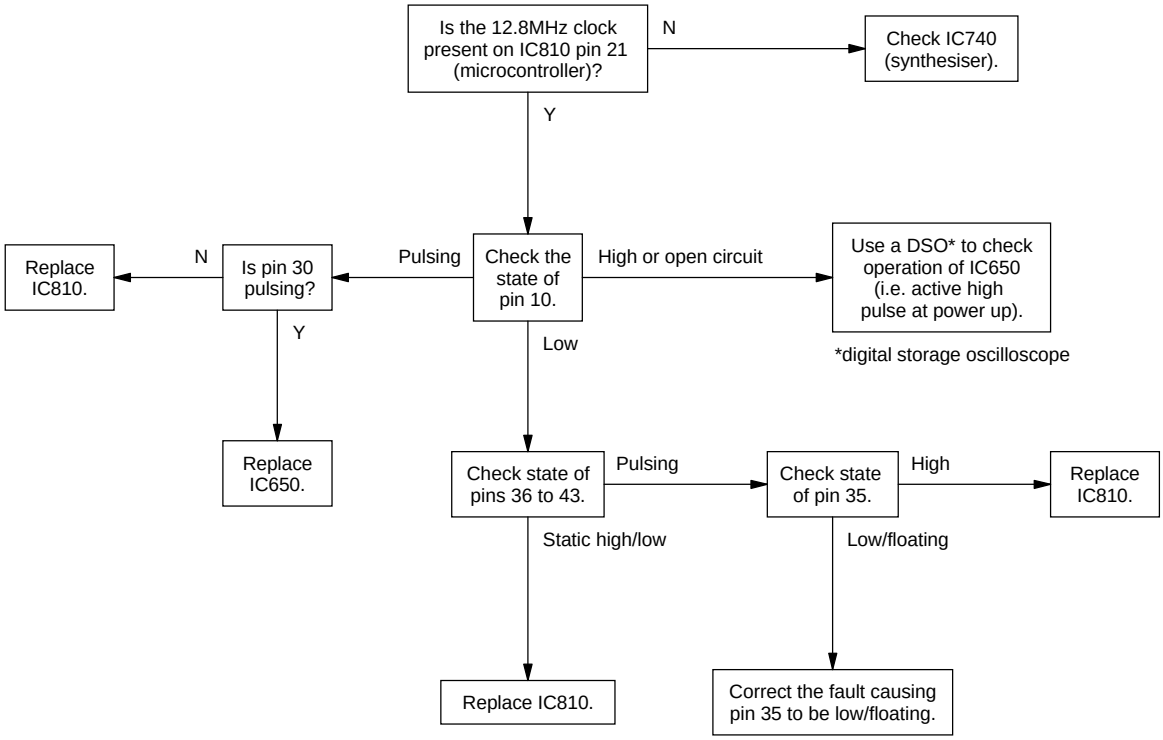
# 5.7 Fault Finding Charts

***Note:*** The standard test point designations used in this section are as follows:

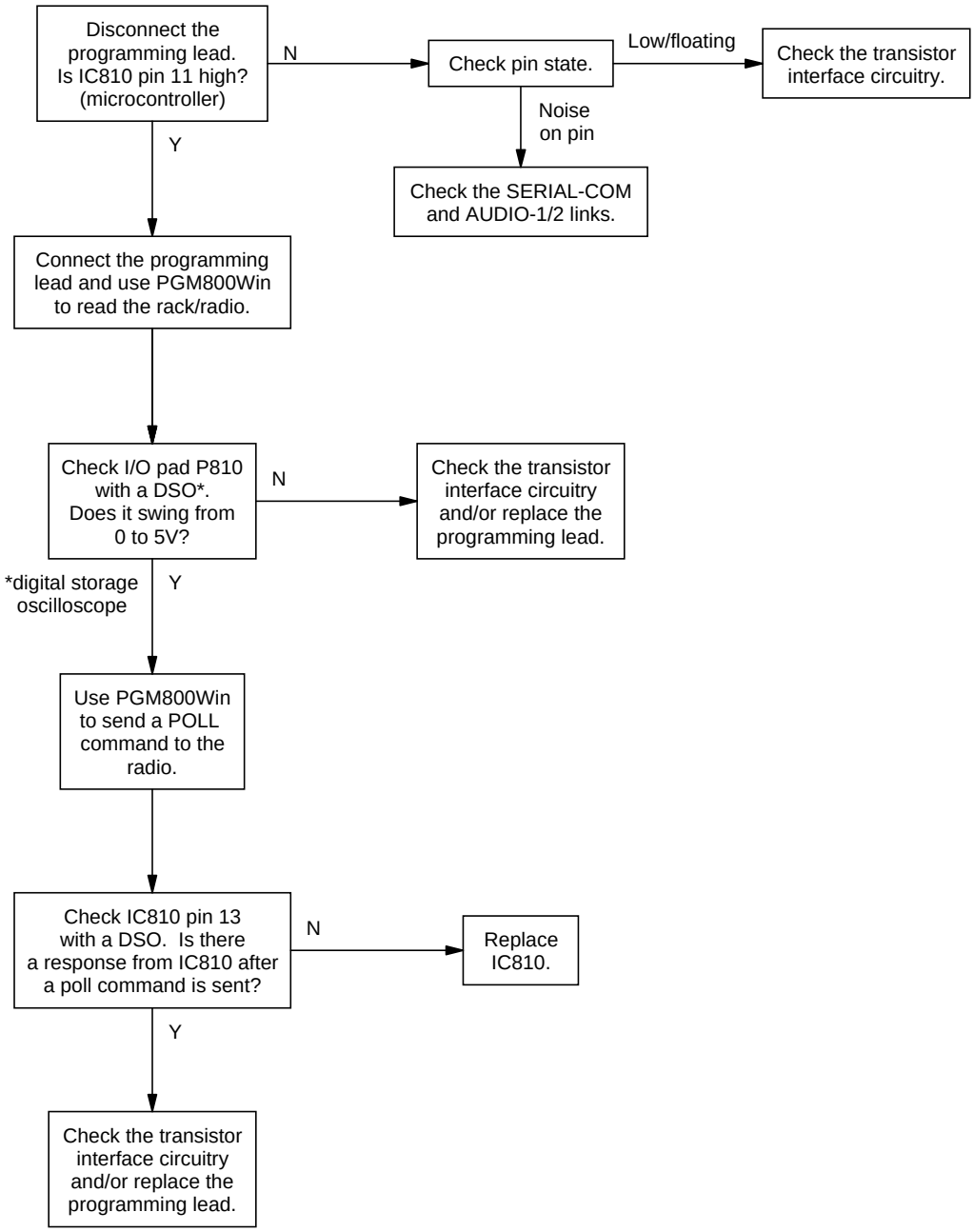
| | |
|---|---|
| TP601 | 13.8V |
| TP602 | 9V |
| TP603 | 20V |
| TP604 | 5V |

## 5.7.1 Microcontroller (IC810)

### 5.7.1.1 Basic Checks

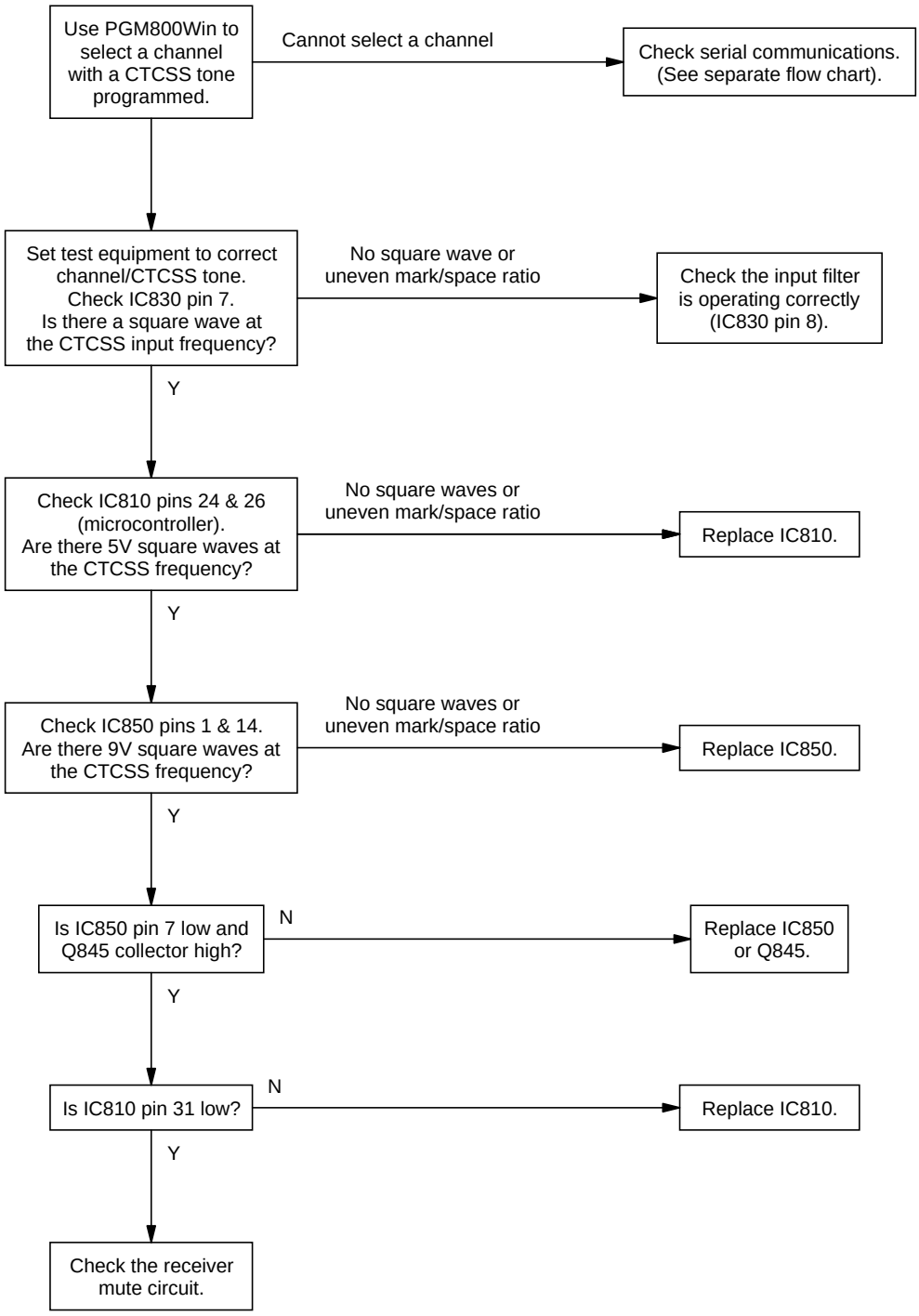


### 5.7.1.2 Serial Communication

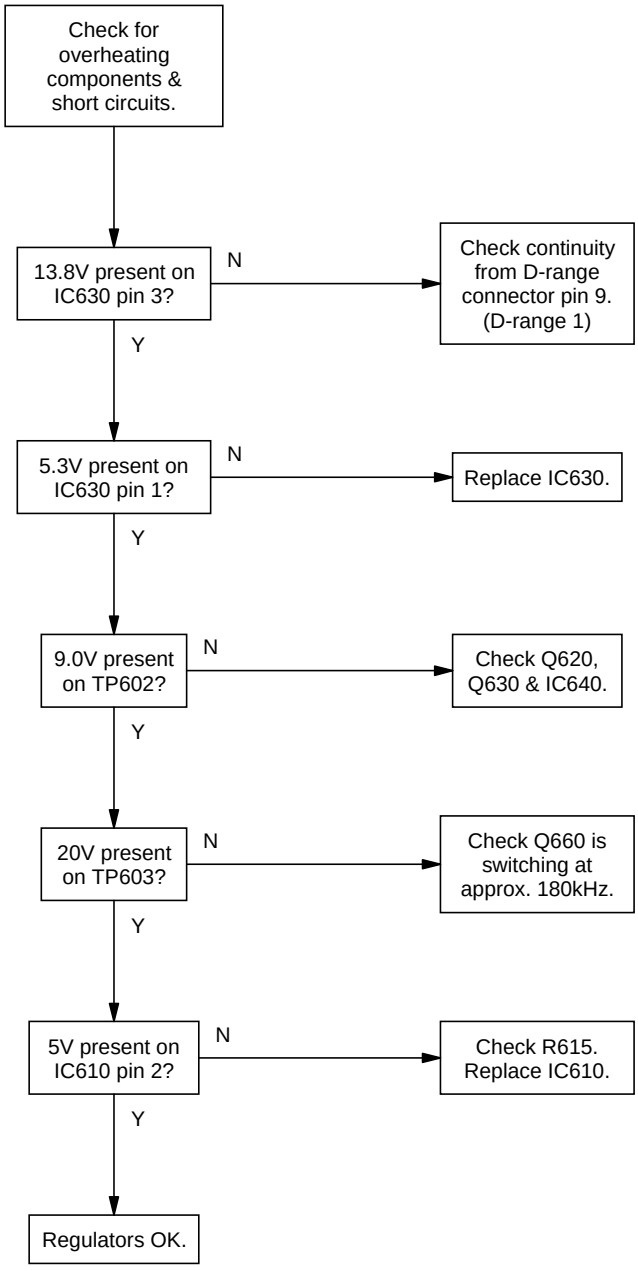


### 5.7.1.3 CTCSS Decode



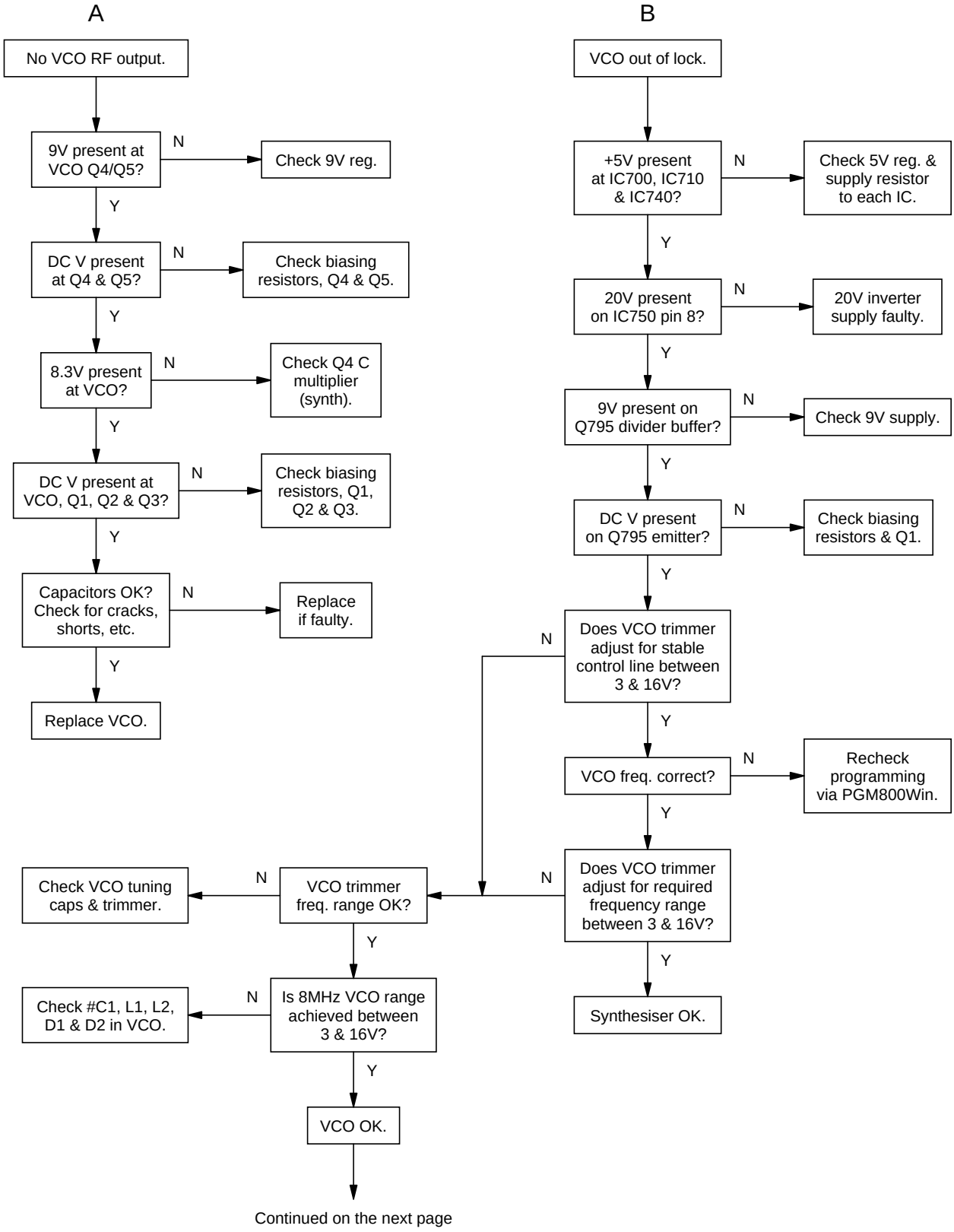
## 5.7.2 Regulator



## 5.7.3 Synthesiser

Refer to the synthesiser circuit diagram (sheet 7) in Section 6 and the VCO circuit diagram in Part E.

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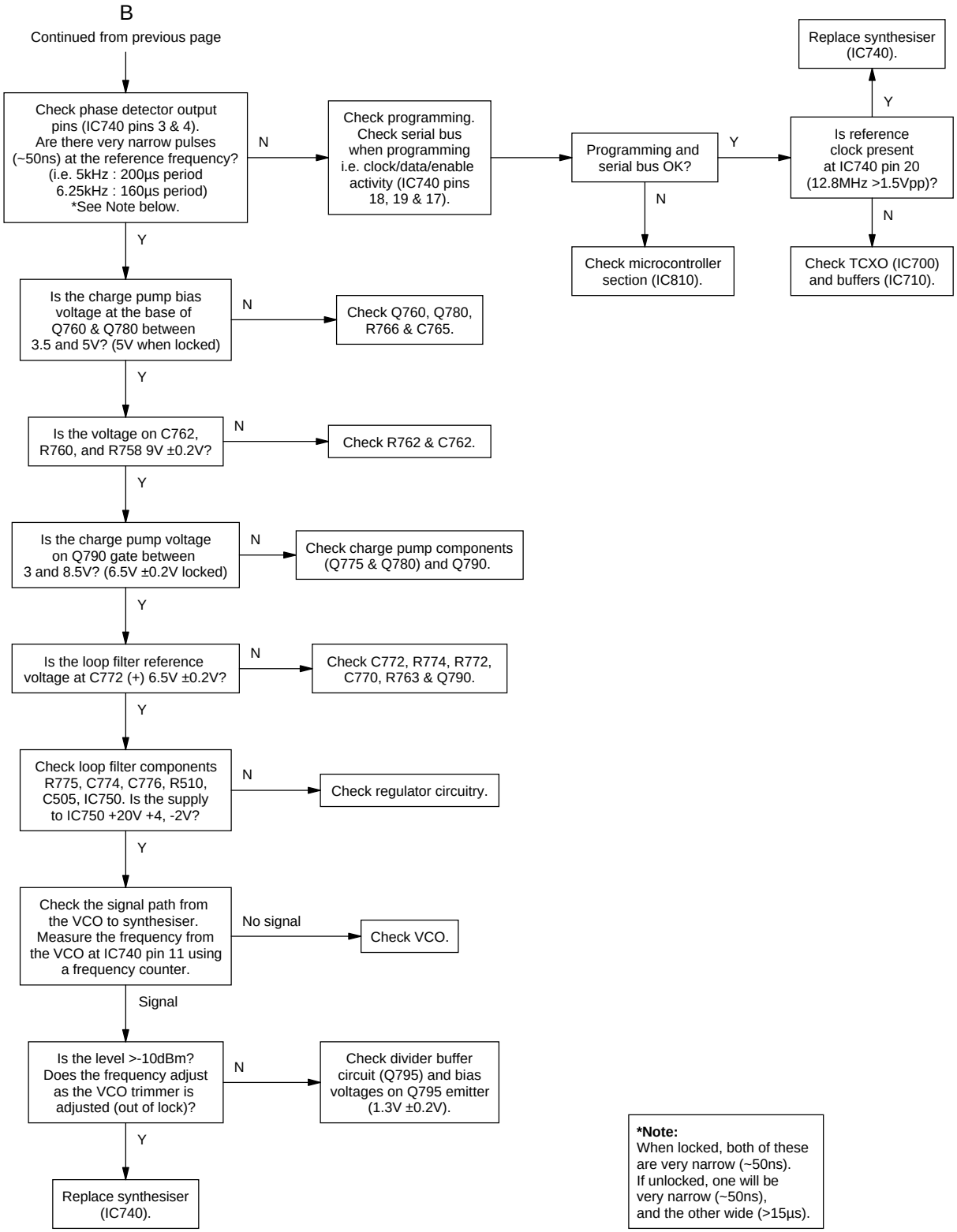
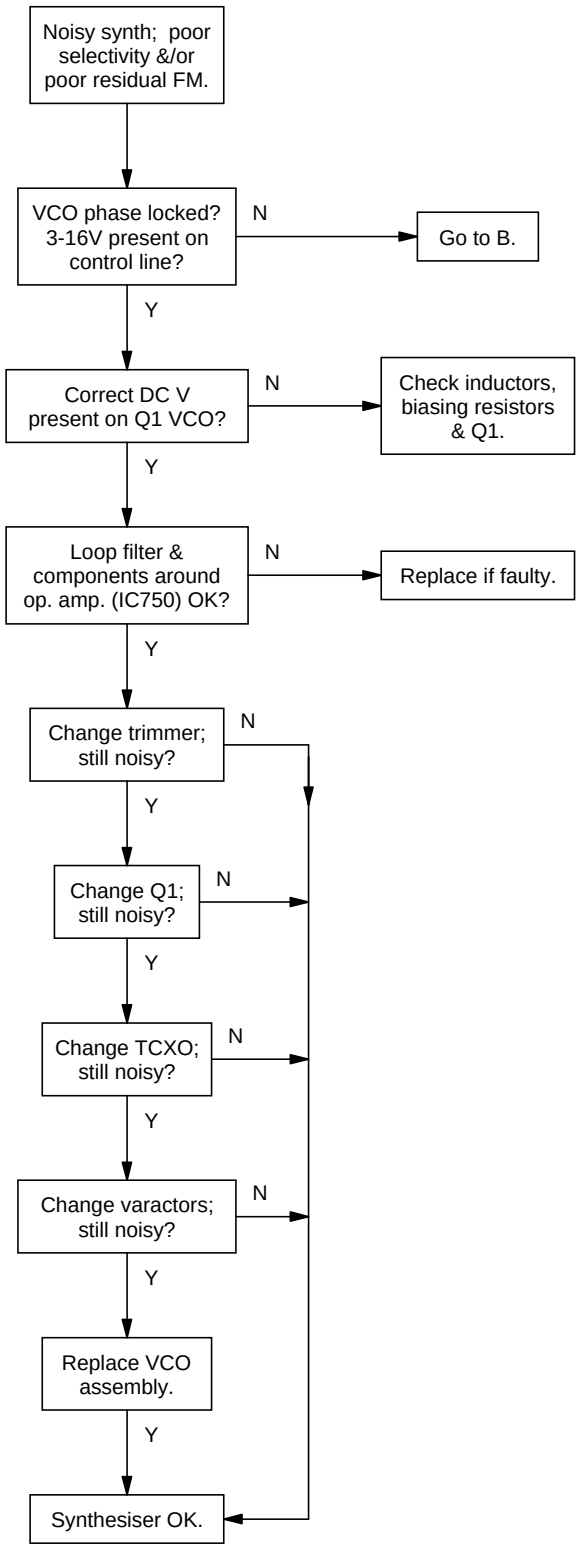
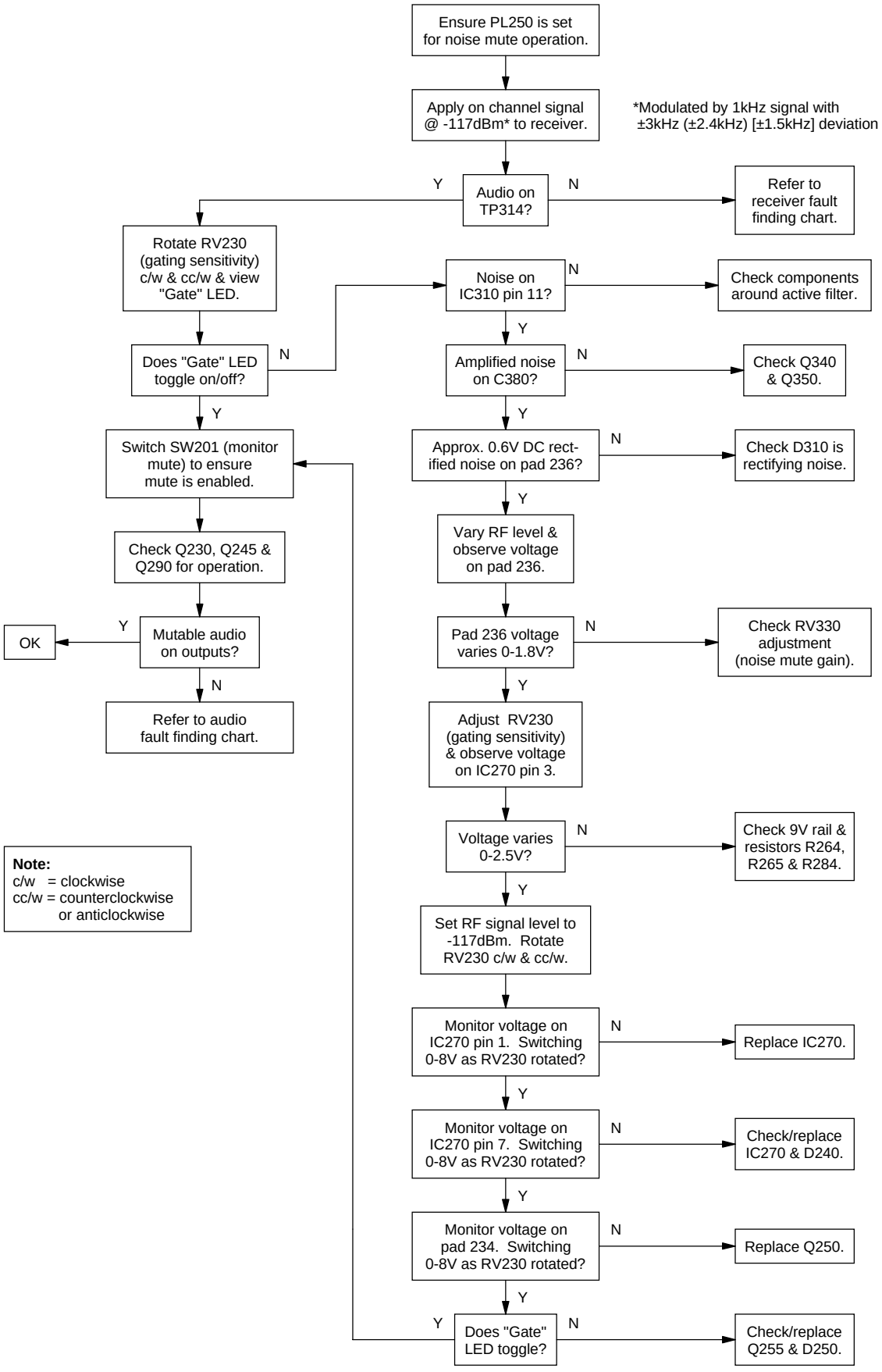


C

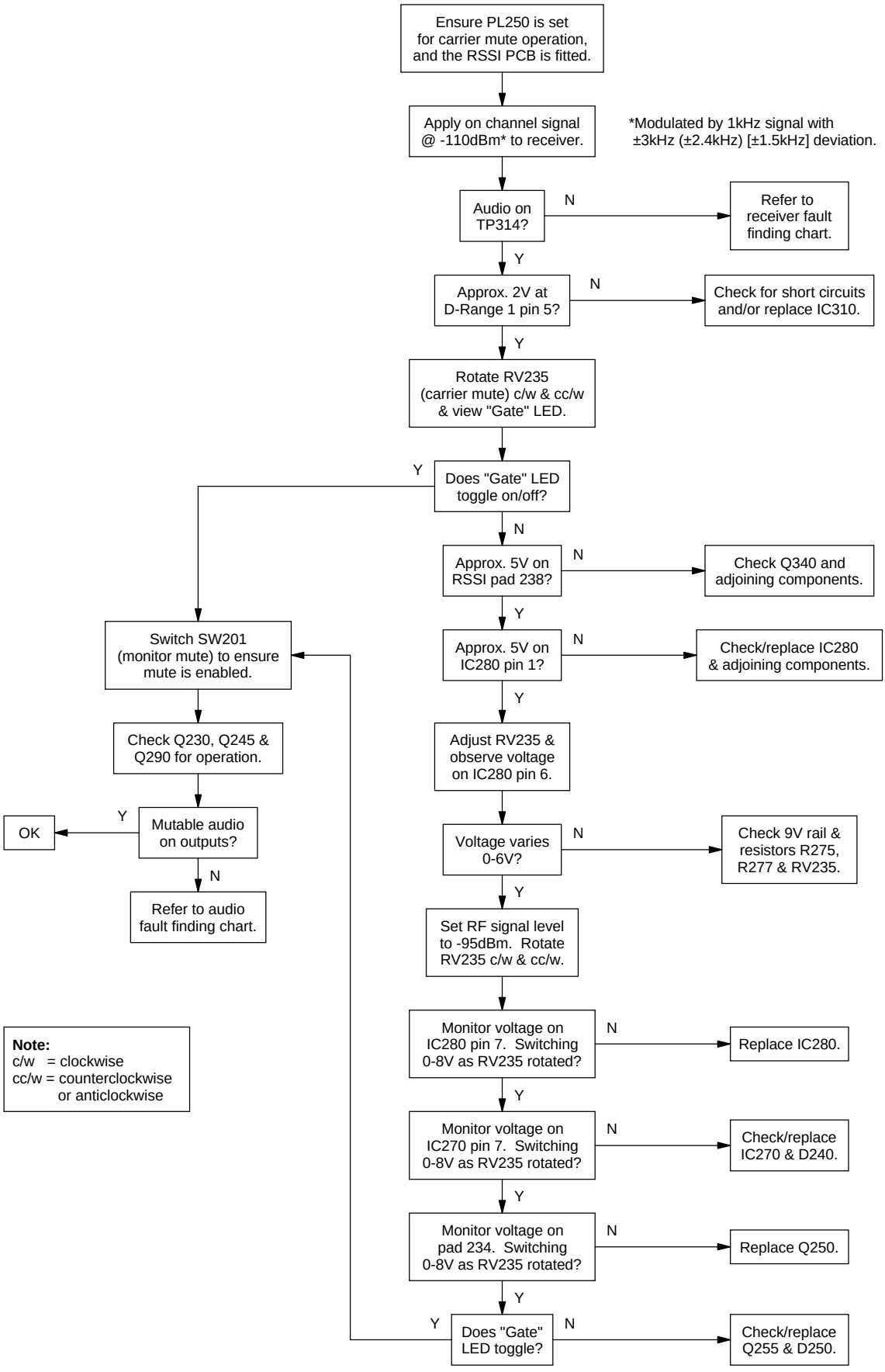

Noisy synth; poor selectivity &/or poor residual FM.
VCO phase locked? 3-16V present on control line?
N
Go to B.
Y
Correct DC V present on Q1 VCO?
N
Check inductors, biasing resistors & Q1.
Y
Loop filter & components around op. amp. (IC750) OK?
N
Replace if faulty.
Y
Change trimmer; still noisy?
N
Y
Change Q1; still noisy?
N
Y
Change TCXO; still noisy?
N
Y
Change varactors; still noisy?
N
Y
Replace VCO assembly.
Y
Synthesiser OK.

## 5.7.4 Noise Mute



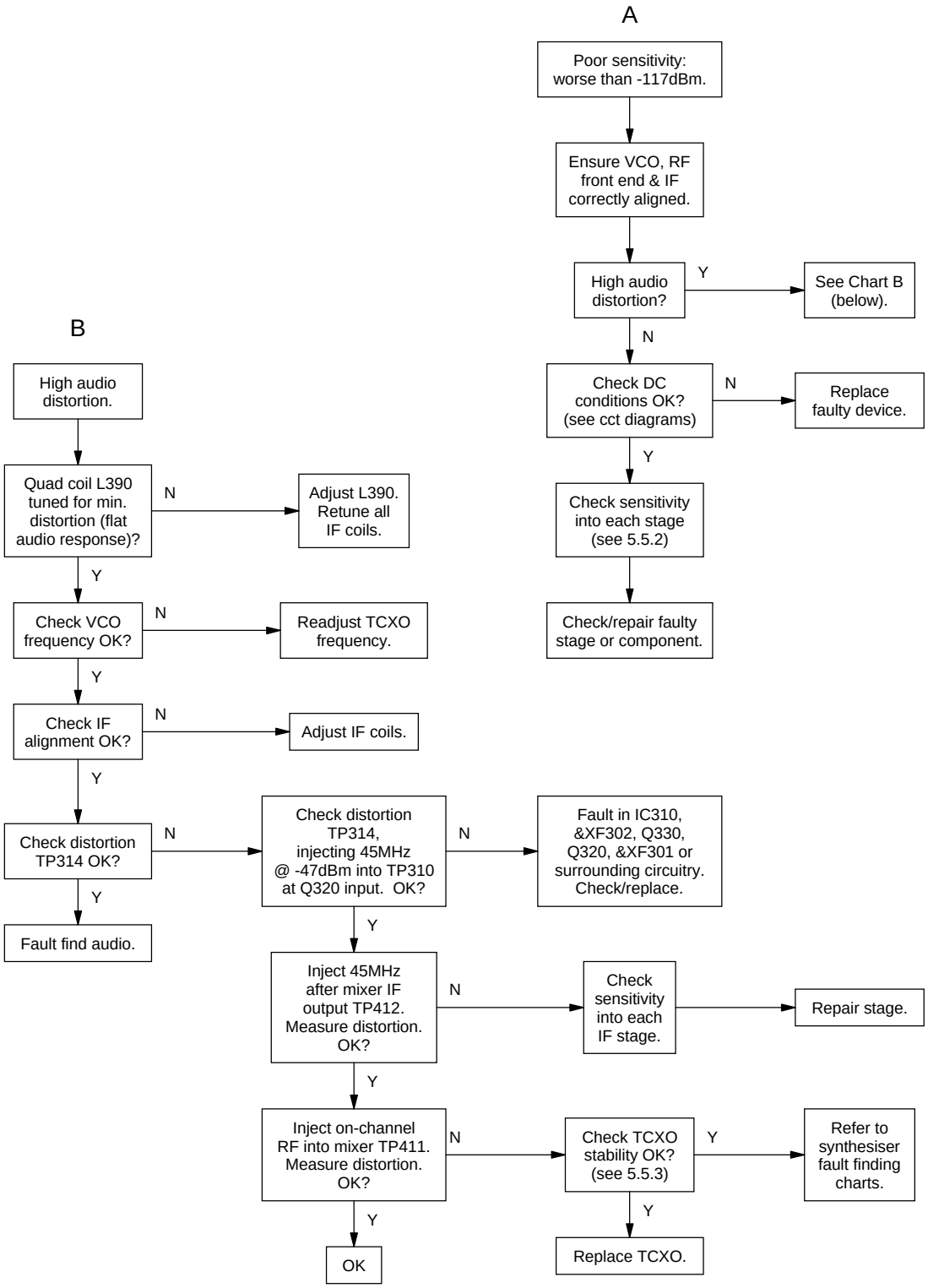

 

## 5.7.5 Carrier Mute



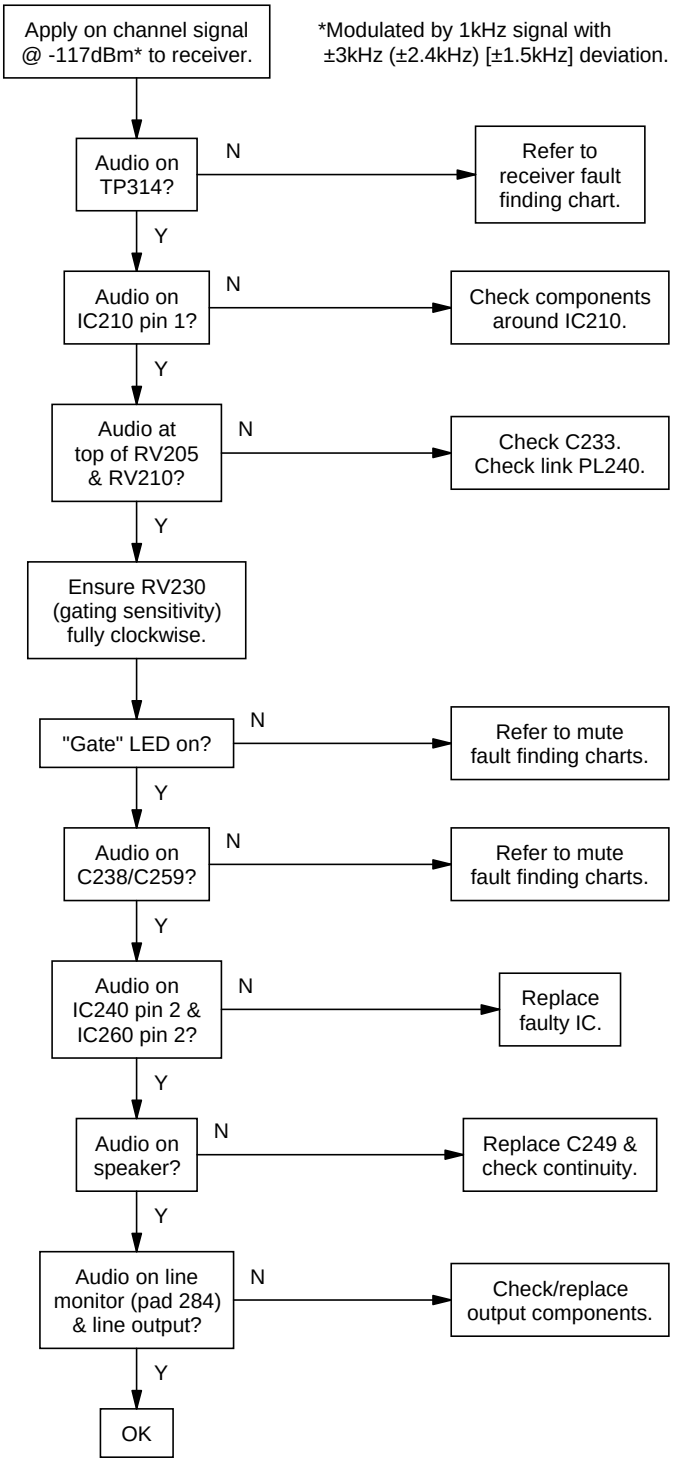
## 5.7.6 Receiver

Refer to the receiver IF and front end circuit diagrams (sheets 3 & 4) in Section 6.



## 5.7.7 Audio


Apply on channel signal @ -117dBm* to receiver.
*Modulated by 1kHz signal with ±3kHz (±2.4kHz) [±1.5kHz] deviation.
Audio on TP314?
N
Refer to receiver fault finding chart.
Y
Audio on IC210 pin 1?
N
Check components around IC210.
Y
Audio at top of RV205 & RV210?
N
Check C233. Check link PL240.
Y
Ensure RV230 (gating sensitivity) fully clockwise.
"Gate" LED on?
N
Refer to mute fault finding charts.
Y
Audio on C238/C259?
N
Refer to mute fault finding charts.
Y
Audio on IC240 pin 2 & IC260 pin 2?
N
Replace faulty IC.
Y
Audio on speaker?
N
Replace C249 & check continuity.
Y
Audio on line monitor (pad 284) & line output?
N
Check/replace output components.
Y
OK